Customer No.: 31561
Docket No.: 12386-US-PA
Application No.: 10/707,865

## REMARKS

**Present Status of the Application**

The Office Action rejected all presently-pending claims 1-14. Specifically, the Office Action rejected claims 1-2, 4-5, 8-10, 12-14 under 35 U.S.C. 102(b), as being anticipated by Nagase et al. (U.S. 6,483,185). The Office Action rejected claims 3 and 11 under 35 U.S.C. 103(a) as being unpatentable over Nagase. The Office Action also rejected claims 6 and 7 under 35 U.S.C. 103(a) as being unpatentable over Nagase in view of Shinohara (U.S. 6, 787,900).

Applicants have amended claims 1, 4, 9 and 12 and cancelled claims 3, 5, 11 and 13 to overcome the rejection. Applicants have also added claims 15-21. The limitations added in claims are described at paragraphs [0023], [0024] and no new matter is entered. After entry of the foregoing amendments, claims 1-2, 4, 6-10, 12, 14-21 remain pending in the present application, and reconsideration of those claims is respectfully requested.

**Discussion of Office Action Rejections**

*The limitations in claims 3 and 11 have been incorporated into claims 1 and 9, respectively. Applicants respectfully traverse the rejection of claims 3 and 11 under 35 U.S.C. 103(a) as being unpatentable over Nagase because a prima facie case of obviousness has not been established by the Office Action*

To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must

teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must " be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

The present invention is in general related a chip package structure and a substrate structure, as claims 1 and 9 recite:

Claim 1. A chip package structure, comprising:

a substrate, having a lateral surface, a first surface and a second surface, wherein the substrate further has a first metallic layer, a second metallic layer and a conductor with the first metallic layer located on the first surface of the substrate, the second metallic layer located on the second surface of the substrate and ***the conductor located on the lateral surface of the substrate*** and the first metallic layer is electrically connected to the second metallic layer through the conductor, ***wherein the conductor has a thickness ranging from 0.1μm to 5μm***;

a lead frame, located on the first surface of the substrate, wherein the lead frame is electrically connected to the first metallic layer;

a first chip, having a first active surface and a first back surface, wherein the first back surface of the first chip is bonded either onto the surface of the lead frame or onto the first surface, and the first chip has a plurality of first bonding pads on the first active surface;

a plurality of first bonding wires, connecting the first bonding pads of the first chip to the lead frame;

a heat sink, located on the second surface and electrically connected to the second metallic layer; and

a packaging material, encapsulating the first chip, the first bonding wires and a portion of the lead frame, the lead frame having another portion exposed to the ambient.

Claim 9. A substrate structure with a lateral surface, a first surface and a second surface, comprising:

a first metallic layer, located on the first surface of the substrate;

a second metallic layer, located on the second surface of the substrate; and

***a conductor, located on the lateral surface of the substrate,*** wherein the first metallic layer is electrically connected to the second metallic layer through the conductor, ***and the conductor has a thickness ranging from 0.1μm to 5μm.***

Nagase fails to teach or suggest that the conductor located on the lateral surface of the substrate has a thickness ranging from 0.1μm to 5μm. In Nagase's reference, as shown in Fig. 9A and Fig.9B, the metal frame 72 is formed to surround all the periphery of the substrate 11 and is shaped by punching a sheet material having a thickness equal to or slightly smaller that the substrate to have the same thickness as the substrate 11 (col. 14, lines 44-54). In particular, Nagase also discloses the substrate 11 has a thickness of 0.635 mm (col. 9, lines 39-40). Therefore, the metal frame 72 formed on the lateral surface of substrate 11 has a thickness about 0.635 mm. However, in claims 1 and 9 of the present invention, the conductor located on the lateral surface of the substrate has a thickness ranging from 0.1μm to 5μm that is much smaller than 0.635 mm. Therefore, Nagase does not teach or suggest each and every element in the claims.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 and 9 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2, 4-5, 8, 10, 12-14 patently define over the prior art as well.

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*Applicants respectfully traverse the rejection of claims 6 and 7 under 35 U.S.C. 103(a) as being unpatentable over Nagase in view of Shinohara (U.S. 6, 787,900) because a prima facie case of obviousness has not been established by the Office Action.*

Applicants submit that, as disclosed above, Nagase fails to teach or suggest each and every element of claim 1, from which claims 6-7 depend. Shinohara also fails to teach or suggest that the conductor located on the lateral surface of the substrate has a thickness ranging from 0.1μm to 5μm. Shinohara cannot cure the deficiencies of Nagase. Therefore, independent claim 1 is patentable over Nagase and Shinohara. For at the least the same reasons, its dependent claims 6-7 are also be patentable.

Applicants further added claims 15-21. In Nagase and Shinohara references, the limitations in claims 15-21 are not disclosed. In particular, the feature in the independent claim 19 comprises the conductor on the lateral surface of the substrate is formed by using sputtering, evaporation plating, chemical vapor deposition, electroplating or coat-spreading, and that is not disclosed by Nagase and Shinohara. Because the conductor is formed by using sputtering, evaporation plating, chemical vapor deposition, electroplating or coat-spreading, the conductor has a thickness ranging from 0.1μm to 5μm (as claim 20 recites). The conductor having a thickness ranging from 0.1μm to 5μm is much smaller than 0.635 mm disclosed by Nagase.

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**CONCLUSION**

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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